

PADS to ADIVA Interface (Quick-Start User Guide)

Notice

Representations in this User Guide are meant as an overview and quick reference. Full details can be found in the On-Line manuals located at the *ADIVA Corporation* website - www.adiva.com

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Getting Started...

- Change PADS database units to either MILS or MM.
- Define Gerber filenames and offsets - place design origin OUTSIDE of all artwork graphics - set artwork "Justification" to "Offset" - enter offset value in MILS or MM (see next slide for greater detail)
- Save Gerber file definitions into PADS database and then output Gerber files.
- Define and separate Drill files into individual files, plated holes, non-plated holes, buried-blind vias.
- Define Drill filenames, set report file to be created in design units, set offsets to same as Gerber, save Drill file definitions into PADS database and then output Drill files.
- Create PADS ascii (jobname.asc) database file in V5.0 format, containing All Data, using current design units set above (either MILS or MM not BASIC).

It is VERY important that the .asc file be created after the Gerber and Drill files have been created and their definitions saved in the PADS database in order for the .asc file to contain the filenames and formats created.

ADIVA will be expecting to sync the filenames in the .asc file to match the actual Gerber and Drill filenames.

NOTE:

- ALL data files (Gerber and Drill along with the .asc file) MUST be of the same units.
- **DO NOT** modify any of the manufacturing filenames after they are created by PADS output or they will be out of sync with the .asc file which will impact the layer recognition and assignment function of the **Pads to Adiva Interface**.

CAM File Offset

Important information regarding data file offsets for Gerber and Drill output

- Adjust the Justification setting in the Options tab for CAM layer setups.
- For a consistent offset for the ADIVA load, The justification option must be set to "offset" and the X Offset: and Y Offset: settings for each layer must match.
- Any other option (in justification) will result in the layers not being aligned when processed.
- Then when going thru the Adiva load, just use the negative equivalent to the PADS offset.

if the offset in Pads (in mils) is X= 1000, Y= 3000

then

the offset in Pads to ADIVA Interface would be X= -1000, Y= -3000

PADS > ADIVA PROCESS

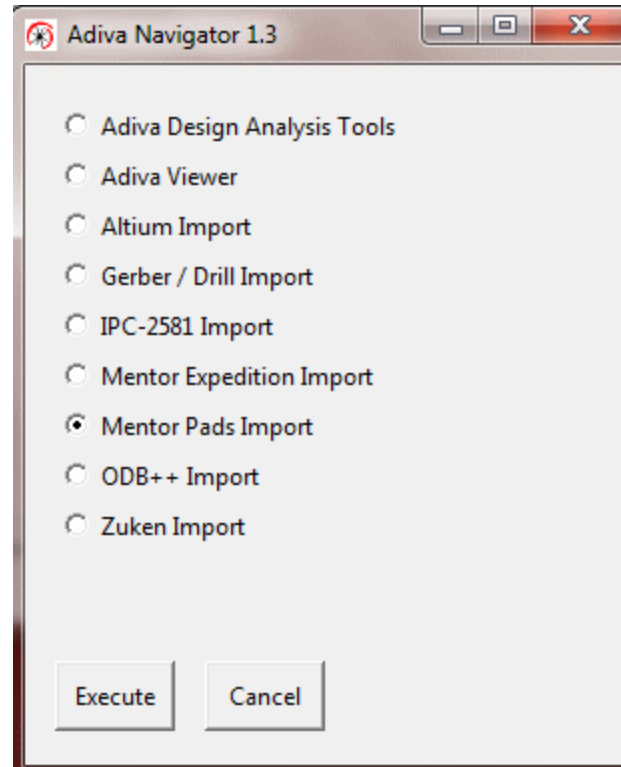
Basic Steps from Start to Finish

- Copy Gerber & Drill & .asc files into the same, clean directory
- Start Interface, choose .asc file from the above directory, setup data formats and define any offsets if required
- Verify / Modify Layer Assignments
- Verify Layer Description
- Extract a Netlist from Manufacturing Data
- Perform Netlist Compare using CAD Netlist against Mfg Netlist
- Define Pad and Hole Classes
- Run DRC Checks

Step 1

PADS to ADIVA Interface

If using the **Adiva Navigator**, select the **Mentor Pads Import** to start the data import process...



If not using the **Adiva Navigator**, select the Windows Desktop Shortcut to **AdivaPads**.

Either action will produce the **Pads to Adiva Interface** dialog on the next page...

Choose a .asc file from PADS

Set .asc file units

Set Drill Data format fields. In this case, Absolute,2,4,Trail means....

Absolute coordinate reference
2 leading digits
4 trailing digits
Trailing zero suppression

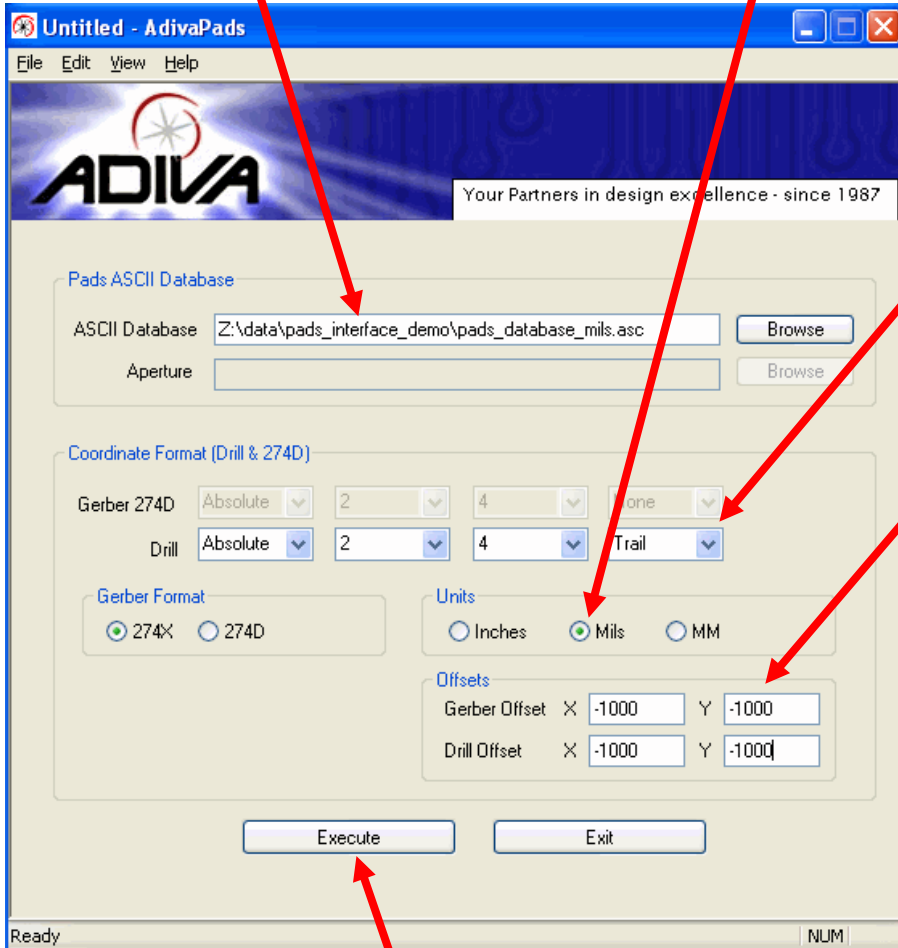
Notice the data file offsets are valued in MILS because the .asc file units value is set to Mils. If the .asc file units are in MM, then these data file offsets need to be in MM units.

Also the values are negative to move Gerber/Drill data back to the CAD system XY values

NOTE:

These default values can be adjusted to reflect your standard settings.

Located in the %ADIVA_DATA% directory (default = c:\adiva\data) is a file named **Pads.fmt**. This file contains the settings that appear by default. Contact ADIVA [support](#) directly for file modification details.



When complete, **Execute** the conversion process

Step 2

Layer Definition Confirmation
and Adjust as Needed

Adjust Layer Names as shown...

If it's a **positive** layer internally – call it an **Inner Circuit**

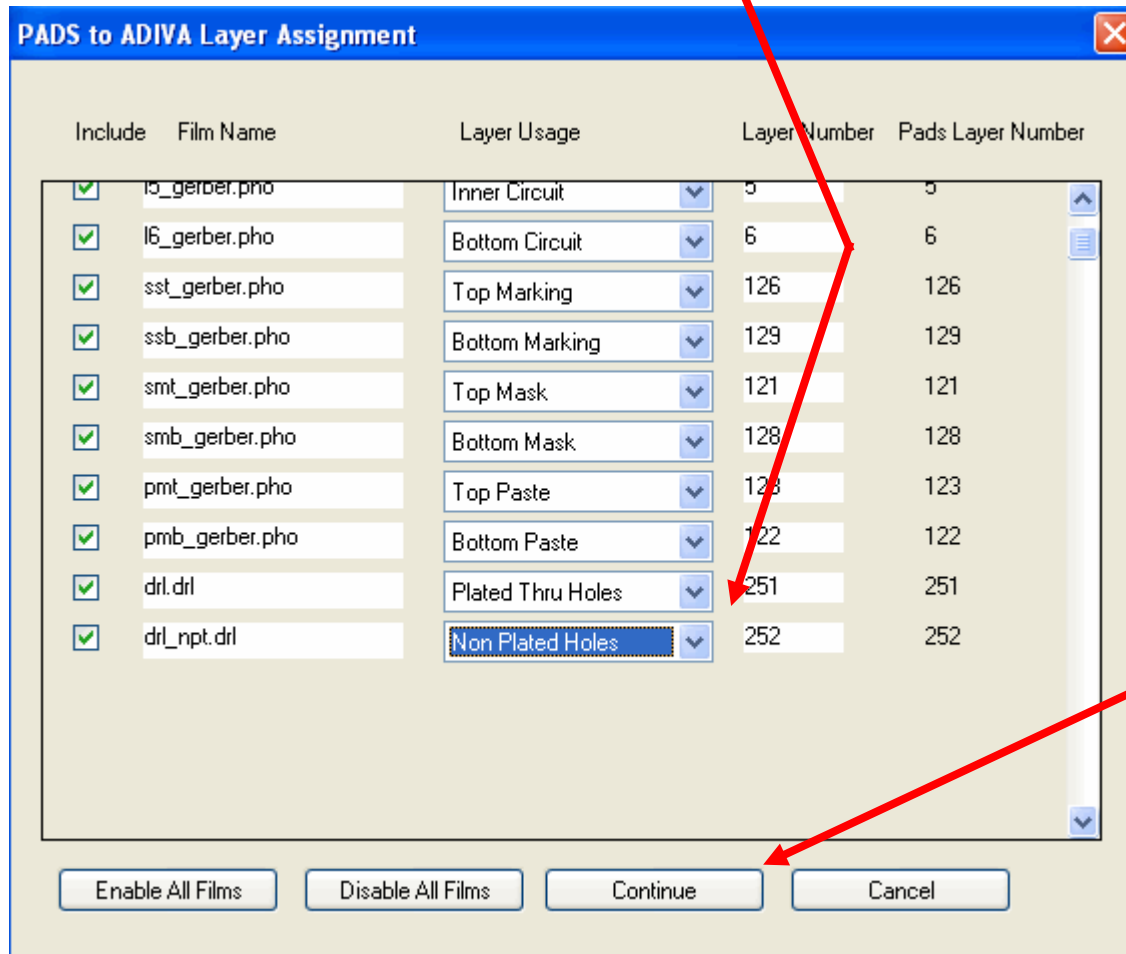
If it's a **negative** layer internally – call it a **Plane**

Uncheck any filename not desired to be converted

Include	Film Name	Layer Usage	Layer Number	Pads Layer Number
<input checked="" type="checkbox"/>	l1_gerber.pho	Top Circuit	1	1
<input checked="" type="checkbox"/>	l2_gerber.pho	Inner Circuit	2	2
<input checked="" type="checkbox"/>	l3_gerber.pho	Inner Circuit	3	3
<input checked="" type="checkbox"/>	l4_gerber.pho	Inner Circuit	4	4
<input checked="" type="checkbox"/>	l5_gerber.pho	Inner Circuit	5	5
<input checked="" type="checkbox"/>	l6_gerber.pho	Bottom Circuit	6	6
<input checked="" type="checkbox"/>	sst_gerber.pho	Top Marking	126	126
<input checked="" type="checkbox"/>	ssb_gerber.pho	Bottom Marking	129	129
<input checked="" type="checkbox"/>	smt_gerber.pho	Top Mask	121	121
<input checked="" type="checkbox"/>	smb_gerber.pho	Bottom Mask	128	128
<input checked="" type="checkbox"/>	pmt_gerber.pho	Top Paste	123	123
<input checked="" type="checkbox"/>	pmb_gerber.pho	Bottom Paste	122	122
<input checked="" type="checkbox"/>	drl.drl	Plated Thru Holes	251	251

Buttons: Enable All Films, Disable All Films, Continue, Cancel

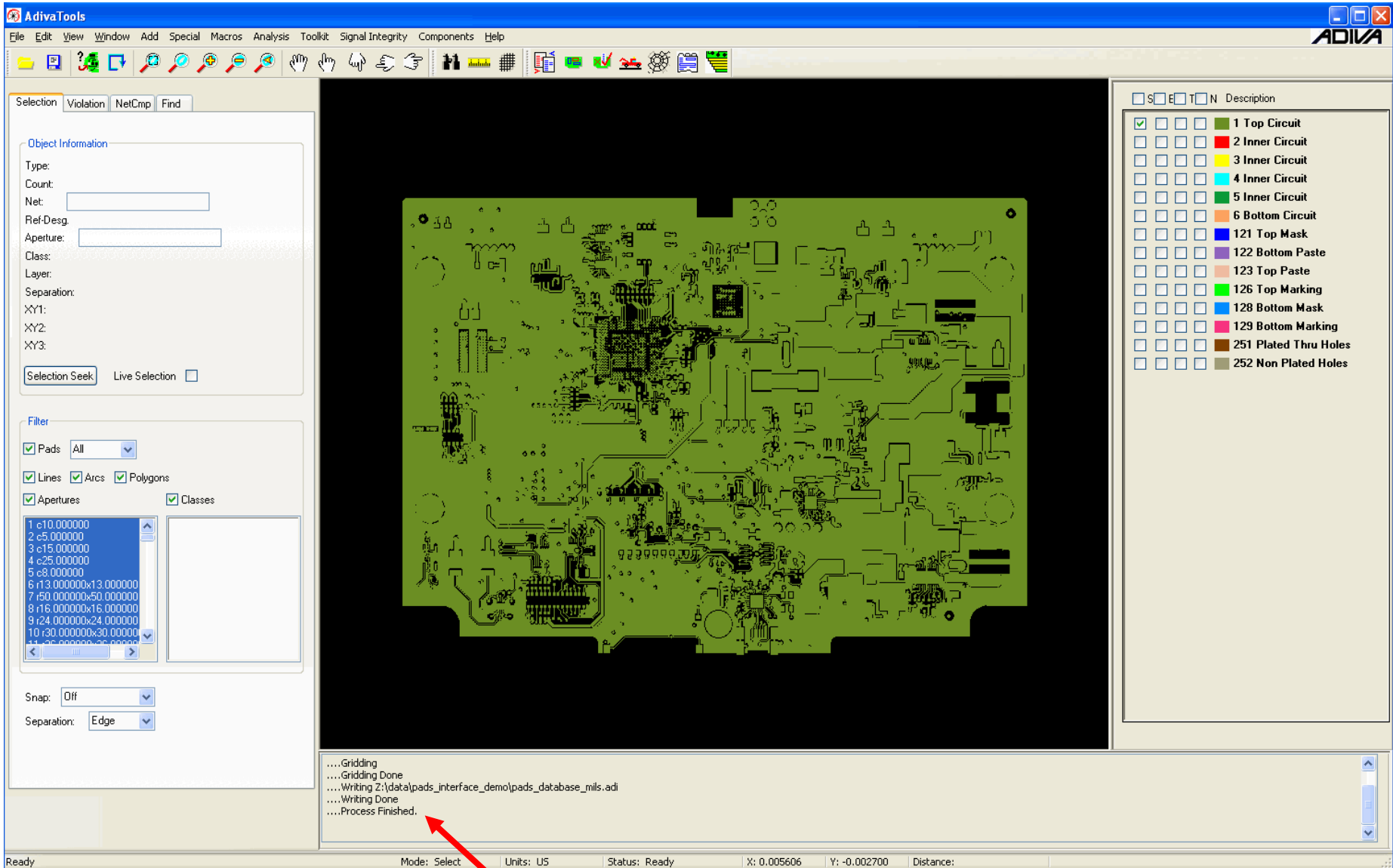
Make sure you check and adjust
Drill Layer names (Plated / Non-Plated)



Select **Continue** to finish
conversion process

Step 3

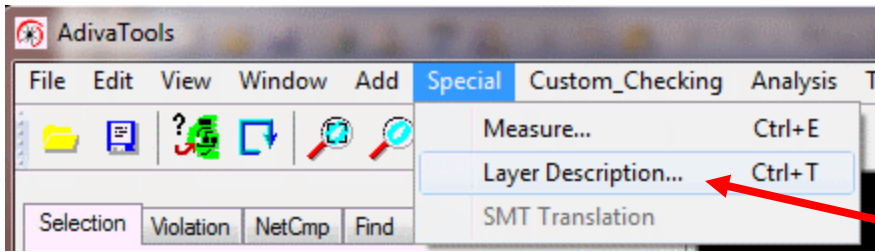
Data Conversion Complete



Database is built and ready for tweaking (if needed) when it says “Process Finished”

Step 4

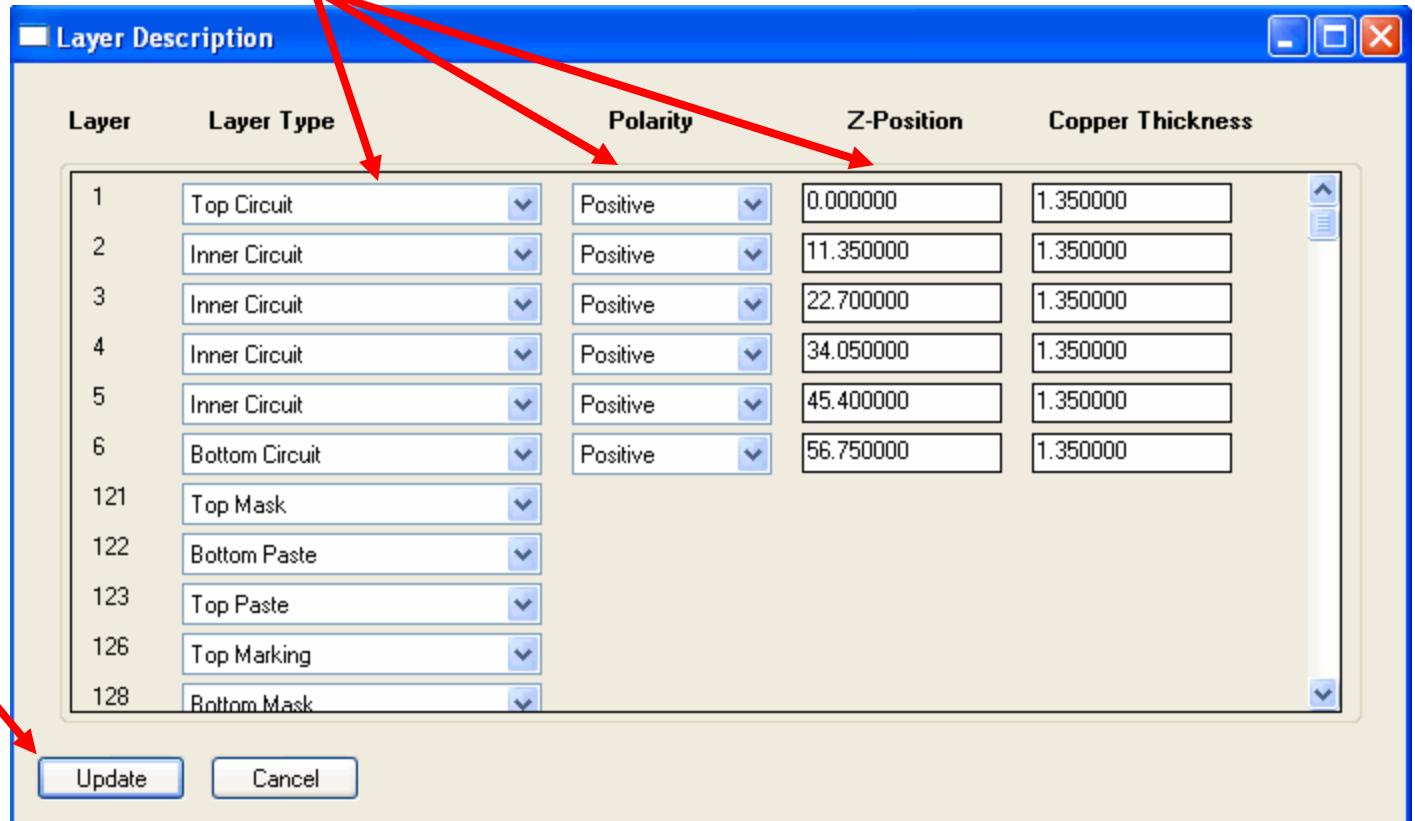
Verify Layer Description



Verify Layer Description Definitions as read and assembled from the .asc file

Choose **Layer Description** from **Special** menu

It is very important to verify “Type”, “Polarity”, “Z-Position” (Z-Position value **MUST** be different for each electrical layer)



Select **Update** when complete

Step 5

Database Preparation - Editing

With a built database, there may be several other functions that need to be completed to prepare a design for DRC analysis. These functions may require some light editing of the data. They include....

Layer Alignment

Board Outline creation

Splitting Non-Plated Holes away from Plated Holes onto their own layer

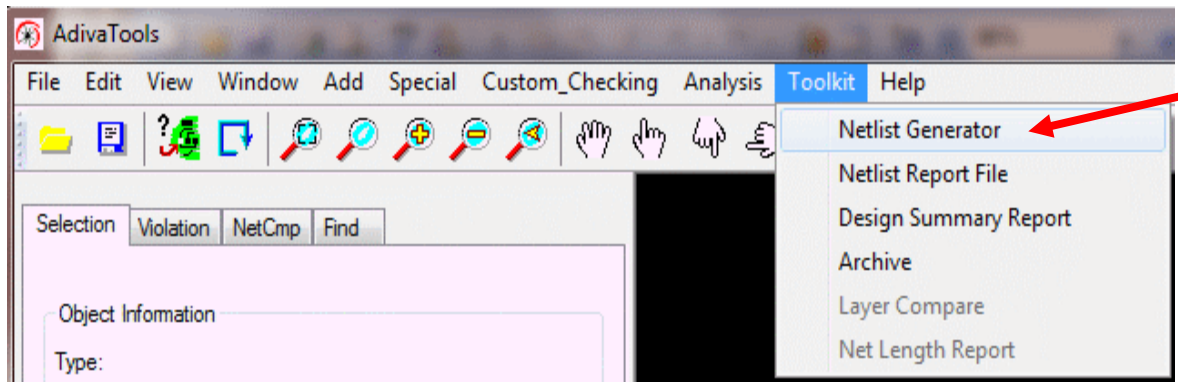
Removing Title Blocks, Coupons, etc

If this is the case, reference the **ADIVA EDITING QUICK-START GUIDE** for details.

Then continue the process of prepping data for analysis....

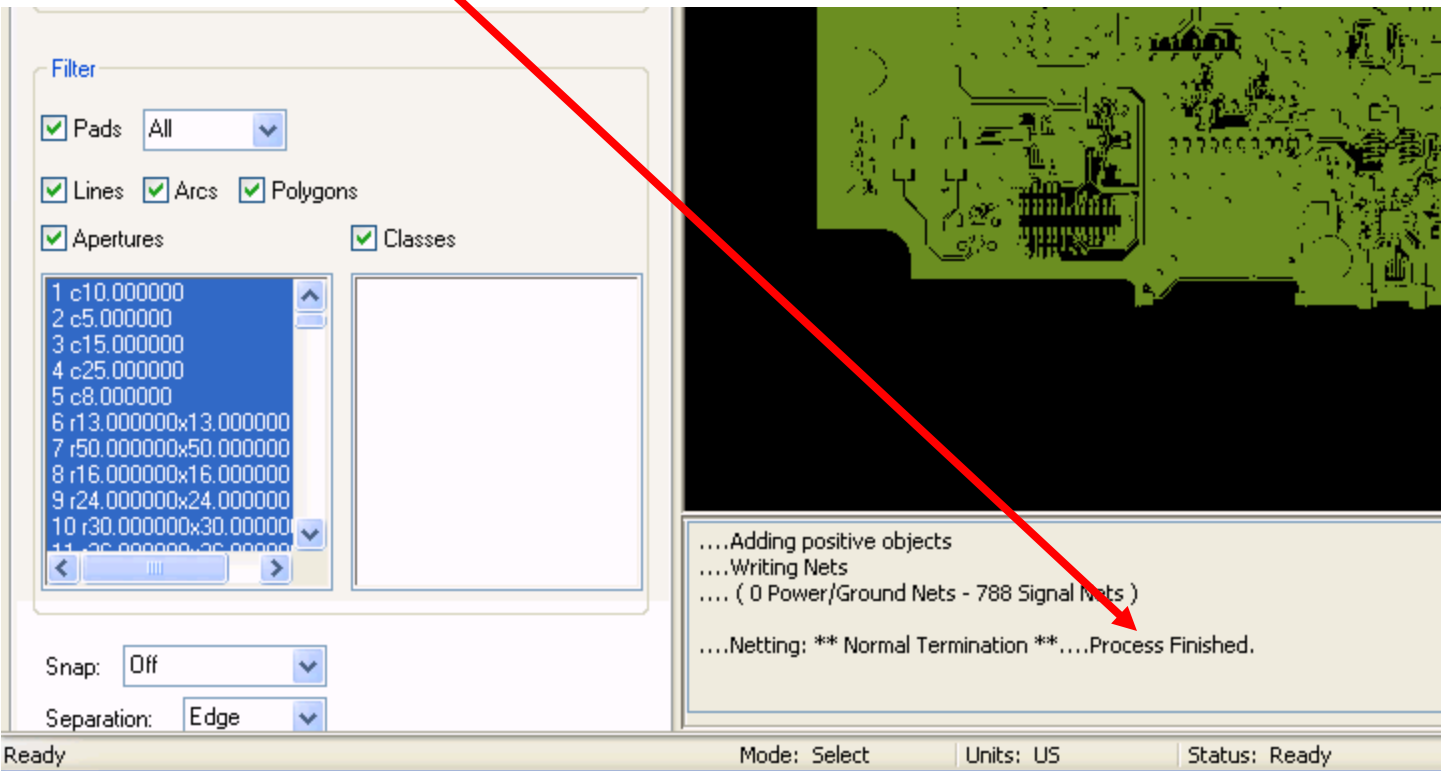
Step 6

Gerber Netlist Extraction



Select **Netlist Generator** from the **Toolkit** menu

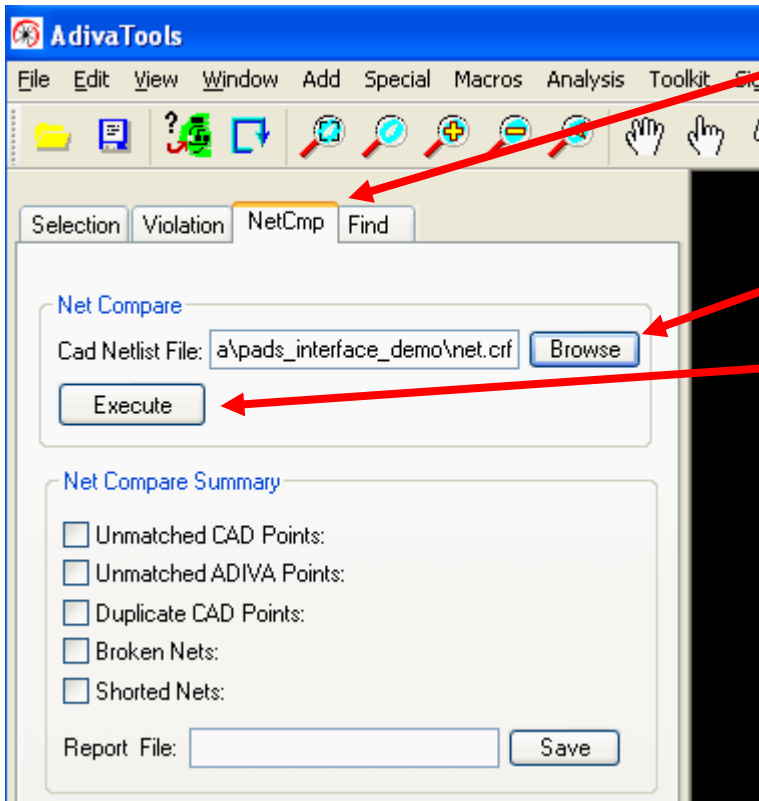
When netting of Gerber is complete, **“Process Finished”** will be displayed in message box



Step 7

Netlist Compare

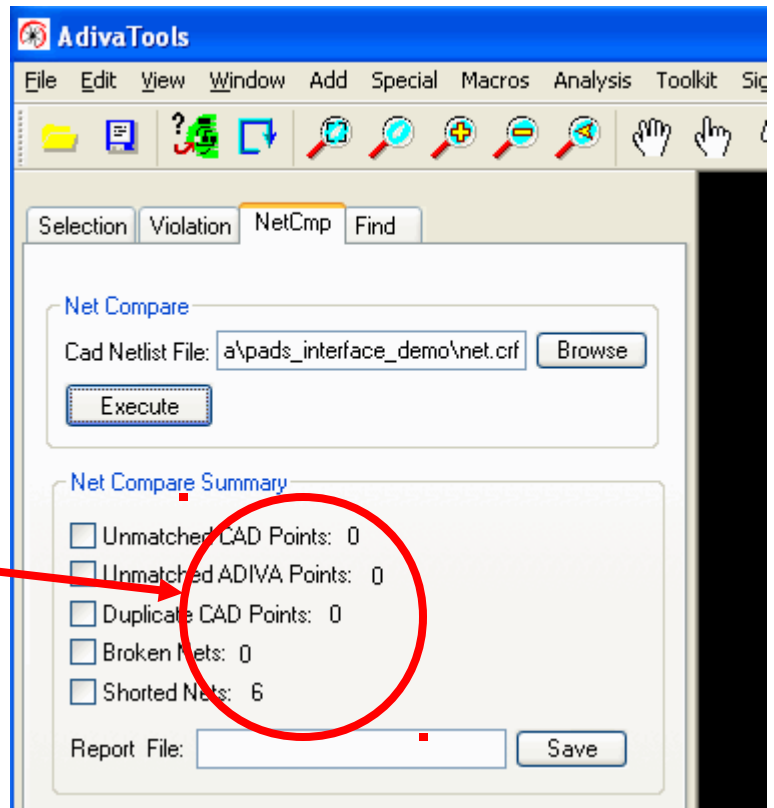
(See the Adiva Netlist Compare Guide
for further details of this process)



Select the **NetCmp** tab

Browse and select the "net.crf" file for this job

Execute the Net Compare Routine



When Net Compare completes, a summary will appear describing any issues

Step 1: Choose the Summary Item to review

Step 2: Scroll to Review Problems and select one to see

The screenshot shows the AdivaTools software interface. On the left, the 'Net Compare Summary' panel is visible, showing a table of netlist items. The 'Show Errors' button is highlighted. The main workspace displays a PCB layout with a green background and black traces. A red arrow points to a specific pin on the board. On the right, a legend lists various layers and components, with a red arrow pointing to a checkbox for '1 Top Circuit'. The status bar at the bottom shows 'Mode: Zoom', 'Units: US', 'Status: Ready', and coordinates.

Qty	ADIVA Net	Netname
1	166	Unused64
17	119	V_BAT
1	119	Unused250
1	100	Unused66
1	100	Unused248
481	100	AGND
3	100	\$7N460
3	100	\$7N456

S	E	T	N	Description
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	1 Top Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	2 Inner Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	3 Inner Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	4 Inner Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	5 Inner Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	6 Bottom Circuit
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	121 Top Mask
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	122 Bottom Paste
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	123 Top Paste
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	126 Top Marking
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	128 Bottom Mask
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	129 Bottom Marking
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	251 Plated Thru Holes
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	252 Non Plated Holes
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	253 Top Cad
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	254 Bottom Cad
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	255 Hole Cad

Turn on Layer(s)
Redraw or Zoom
if Needed

Step 3: Select "Show Errors"
to get idea where problem is

Highlight toggles on or off the selected netname

Select a pin to bulls-eye its location

AdivaTools
 File Edit View Window Add Special Macros Analysis Toolkit Signal Integrity Components Help

Selection Violation NetCmp Find

Net Compare
 Cad Netlist File: Z:\data\pads_interface_demo\ [Browse]
 [Execute]

Net Compare Summary

- Unmatched CAD Points: 0
- Unmatched ADIVA Points: 0
- Duplicate CAD Points: 0
- Broken Nets: 0
- Shorted Nets: 6

Report File: [] [Save]

Qty	ADIVA Net	Netname
1	18	Unused64
17	115	V_BAT
1	119	Unused250
1	100	Unused66
1	100	Unused248
481	100	AGND
3	100	\$7N460
3	100	\$7N456

[Show Errors] [Highlight]

Pins

```

0.551000 2.592000 J10.4 $7N460 C
2.929100 3.401600 U32.C16 $7N460 C
0.579000 2.881900 R54.1 $7N460 C
  
```

.....Netting: ** Normal Termination **.....Process Finished.
Running Cad Netlist Compare using Z:\data\pads_interface_demo\net.crf
Cad Netlist Compare Done.

Left mouse and drag between two points to pan.

Ready Mode: Zoom Units: US Status: Ready X: 0.753590 Y: 2.776230 Distance:

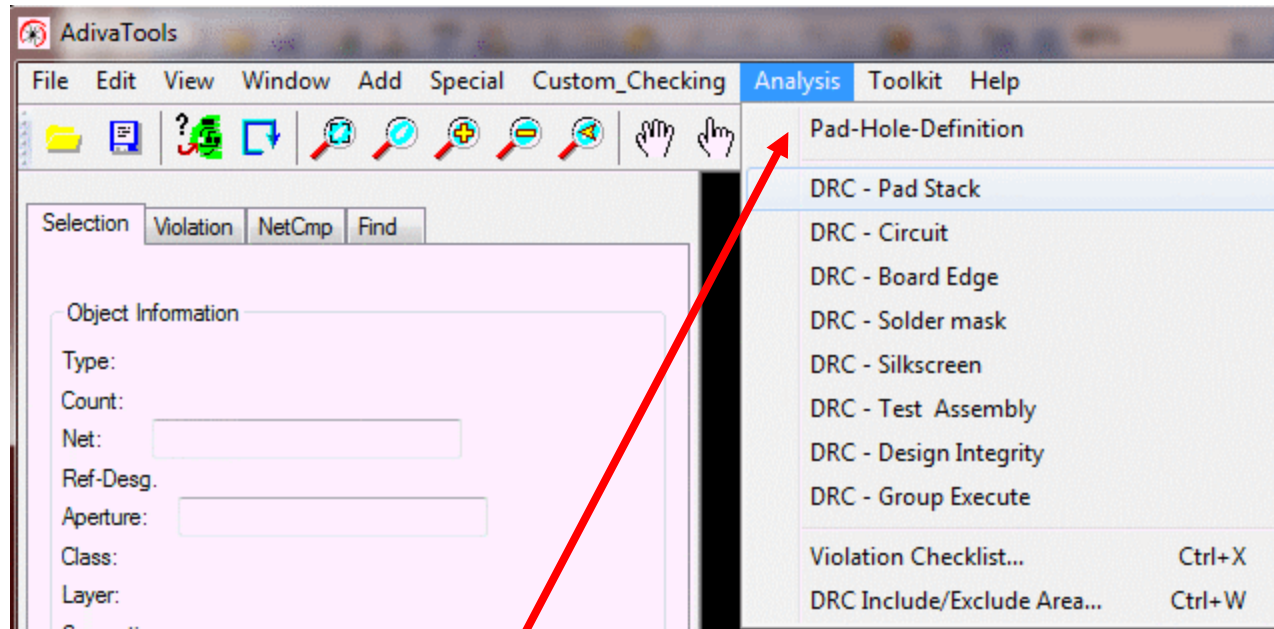
Uncheck All Summary Items to “Exit” Net Compare

Step 8

Pad / Hole Definition

Adds Pad “FUNCTION” Intelligence to
Database

Pad / Hole Definition needed to Identify Pad and Hole types so that various checks can be run accurately

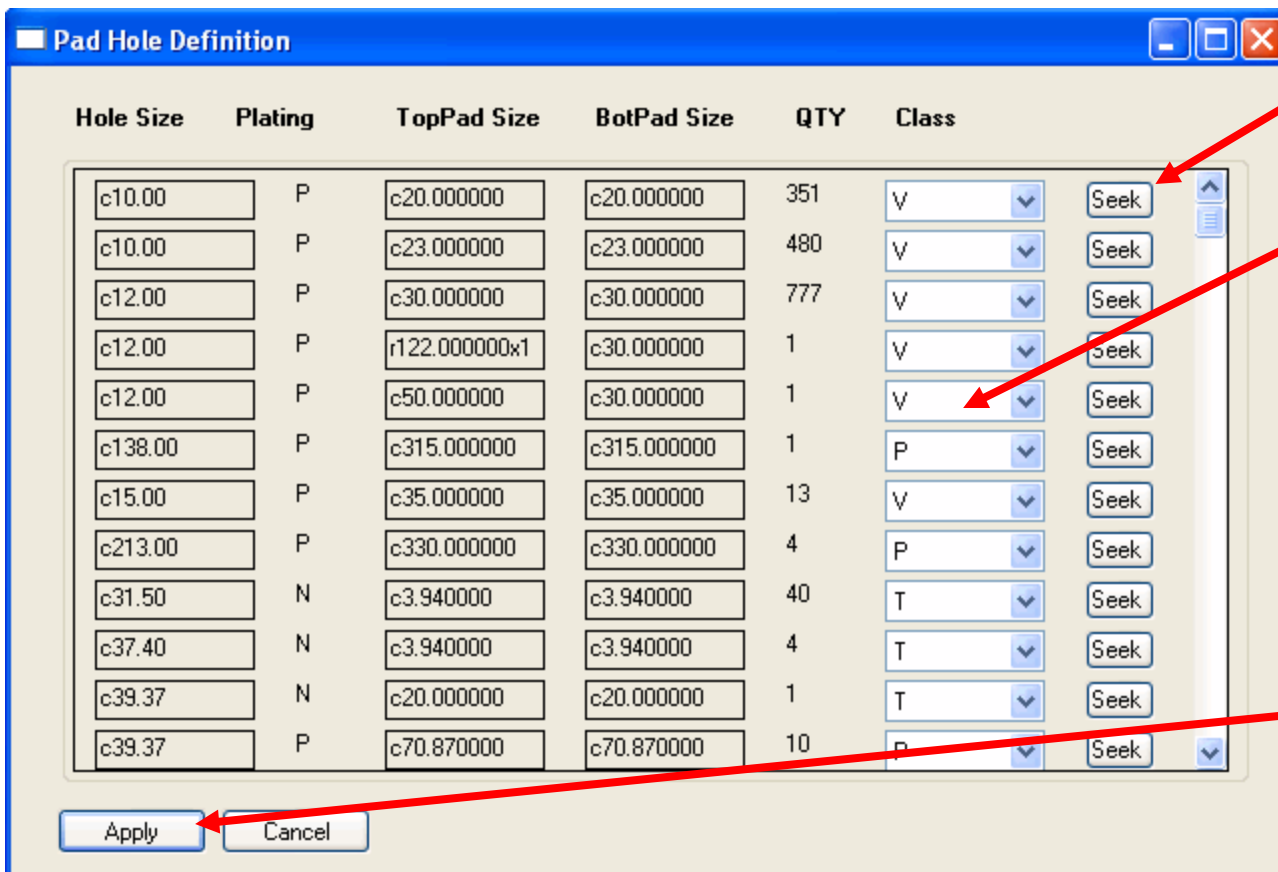


Select **Analysis > Pad-Hole Definition** to start routine

Review the “stackups” that are created by zooming in on Layer 1
 And selecting the “**Seek**” button for each Padstack Type. Watch the screen jump to the next “seek”

NOTE: Only 1 or 2 “seeks” per padstack type should be used to determine if the default choice is correct.

Do a quick glance at each one, adjust if needed (usually not needed) then move on to the next one – don’t let this process take more than a few minutes!



If default choice requires adjustment, adjust as needed to one of the following options...

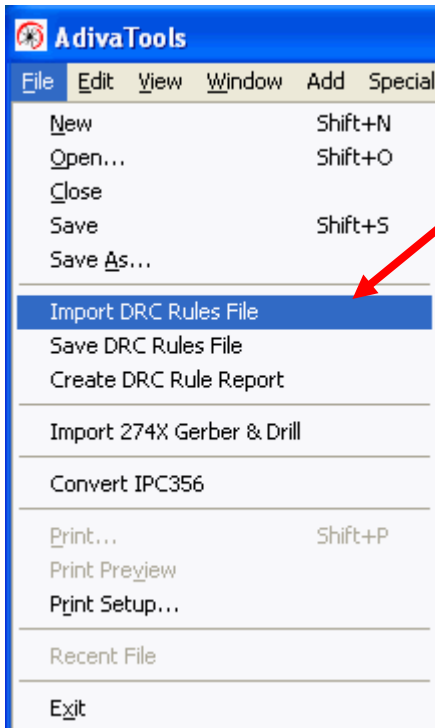
- V = Via
- S = SMT
- P = Pin -Thru hole
- C = Cosmetic (no real function)
- t = test point
- T = Non-Plated Hole
- F = fiducial

Select **Apply** to finish routine

Step 9

Load DRC Check Rules

(See ADIVA DRC Check User Guide for more details)



Select **File > Import DRC Rules** to bring in a master set of rules that you may have created.

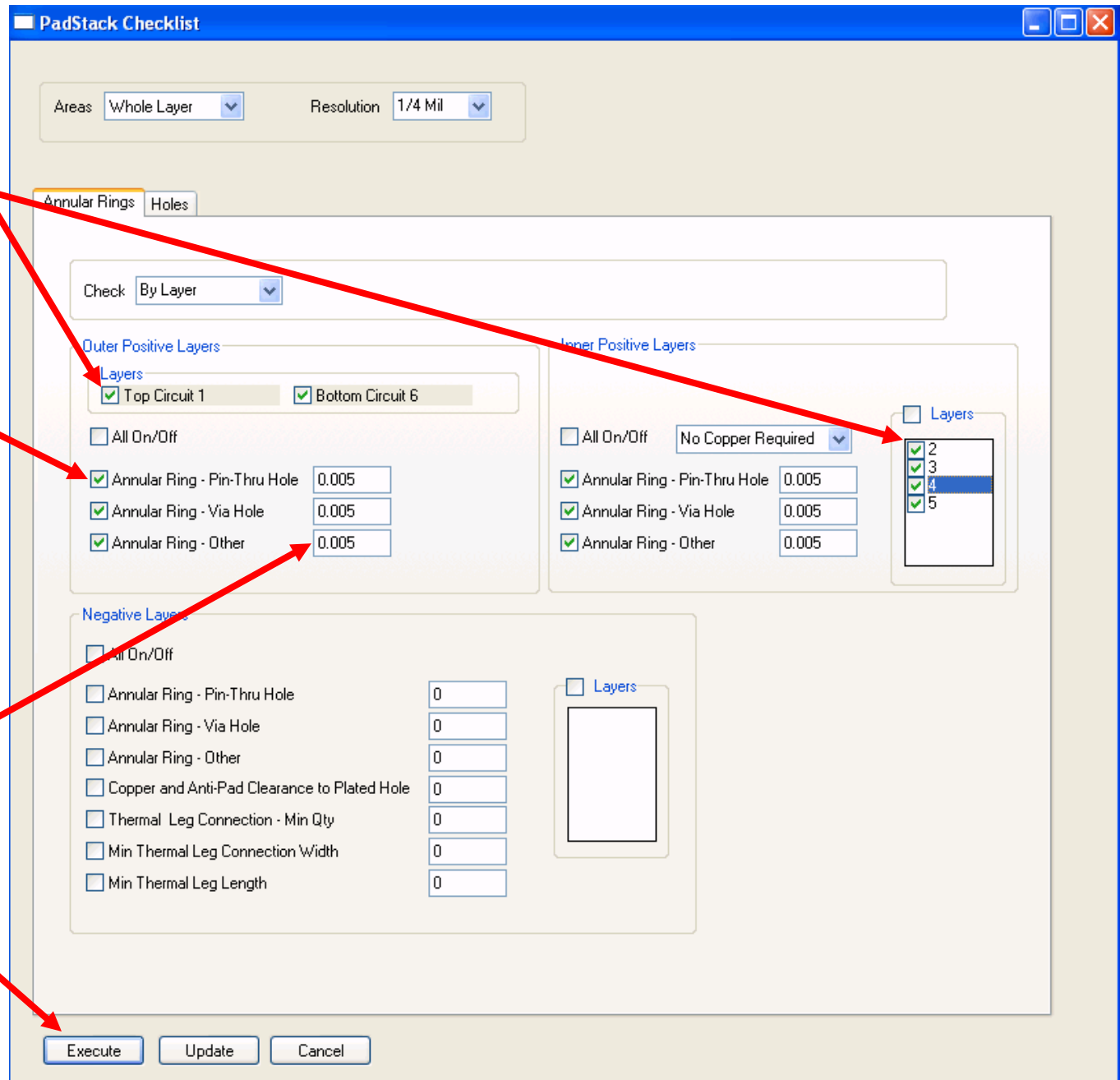
Typically these are stored in the c:\adiva\data directory

In this case, load a file called “**95_example.rul**” which is a basic set of IPC rules and industry standards that ADIVA supplies with all installations.

Step 10

DRC Checks

(See ADIVA DRC Check User Guide for more details)



Check ON layers to review

Check ON checks to run

Values are in inches or mm
5-mil space = 0.005 value

Execute to start checks

Circuit Checklist

Areas: Whole Layer Resolution: 1/4 Mil

Check: By Layer

Outer: Inner NegPlane

Outer Positive Layers

Layers: Top Circuit 1 Bottom Circuit 8

All On/Off

Checks

<input checked="" type="checkbox"/> Min Trace to Trace	0.004	<input checked="" type="checkbox"/> Min SMT to SMT	0.004
<input checked="" type="checkbox"/> Min Trace to Pad	0.004	<input checked="" type="checkbox"/> Min SMT to SMT (Same Net)	0.004
<input checked="" type="checkbox"/> Min Trace to ViaPad	0.004	<input checked="" type="checkbox"/> Min ViaPad to ViaPad	0.004
<input checked="" type="checkbox"/> Min Trace to SMT	0.004	<input checked="" type="checkbox"/> Min ViaPad to SMT	0.004
<input checked="" type="checkbox"/> Min Trace to TestPad	0.004	<input checked="" type="checkbox"/> Min ViaPad to SMT (Same Net)	0.004
<input checked="" type="checkbox"/> Min Pad to Pad	0.004	<input checked="" type="checkbox"/> Min ViaPad to TestPad	0.004
<input checked="" type="checkbox"/> Min Pad to Pad (Same Net)	0.004	<input checked="" type="checkbox"/> Min TestPad to TestPad	0.004
<input checked="" type="checkbox"/> Min Pad to ViaPad	0.004	<input checked="" type="checkbox"/> Min TestPad to SMT	0.004
<input checked="" type="checkbox"/> Min Pad to TestPad	0.004	<input checked="" type="checkbox"/> Min TestPad to SMT (Same Net)	0.004
<input checked="" type="checkbox"/> Min Pad to SMT	0.004	<input checked="" type="checkbox"/> Min Back-Drill to Trace	0.012
<input checked="" type="checkbox"/> Min Pad to SMT (Same Net)	0.004	<input checked="" type="checkbox"/> Min Back-Drill to Pad (any type)	0.012
<input checked="" type="checkbox"/> Min Copper to Fiducial	0.02	<input checked="" type="checkbox"/> Min Trace Width	0.004
<input checked="" type="checkbox"/> Min Fiducial Barrel	0.02	<input type="checkbox"/> Min Trace Connection Width	
<input checked="" type="checkbox"/> Min Copper to Board Edge	0.02	<input type="checkbox"/> Min Resist Sliver	0
<input checked="" type="checkbox"/> Min Trace to Non-Plated-Hole	0.02	<input checked="" type="checkbox"/> Min Acid Trap <input checked="" type="checkbox"/> Traces Only	3
<input checked="" type="checkbox"/> Min Pad (any type) to Non-Plated-Hole	0.02	<input type="checkbox"/> Min Trace Angle	135

Execute Update Cancel

Some checks don't use mils for a value...

This is pixels

This is degrees

Step 11

Violation Review

(See ADIVA DRC Check User Guide for more details)

The Violation Checklist appears when checks are completed

The Checklist can also be opened while checks are running by selecting its Toolbar Icon



Violations are displayed by concern level as defined by the range setting

Save violations to a file to read back and review later

	Accepted	Param	Layer	Seq	Violation Type	Comment
<input type="checkbox"/>	0	4.00000	4	34	Thermal Leg Connection - Min Qty	
<input type="checkbox"/>	0	4.00000	7	36	Thermal Leg Connection - Min Qty	
<input checked="" type="checkbox"/>	0	0.00500	2	17	Annular Ring - Via Hole	
<input checked="" type="checkbox"/>	0	0.00500	4	18	Annular Ring - Via Hole	
<input checked="" type="checkbox"/>	0	0.00500	7	20	Annular Ring - Via Hole	
<input checked="" type="checkbox"/>	0	4.00000	5	35	Thermal Leg Connection - Min Qty	
<input checked="" type="checkbox"/>	0	0.00500	5	19	Annular Ring - Via Hole	
<input type="checkbox"/>	0	0.00500	2	21	Annular Ring - Other	
<input type="checkbox"/>	0	0.00500	4	22	Annular Ring - Other	

Choose a **Violation Type** and amount to review by using **ViolSeek** on the main user interface

Select **Close Violation Checklist** to close the dialog (violations are not lost)

Adjusting the **Violation Range** effects violation count distribution in the **Violation Checklist**. The values listed for each range analyze how close a violation comes to the parameter to determine the category a particular violation will be placed. Changes take effect on **Update**.

For example.... given the range values shown, if a check parameter is 0.005 and the violation amount is 0.00480 – this violation amount falls within ¼ Mil of the parameter categorizing the violation as “**Tolerance**”. If the violation amount is 0.0046 – this makes the violation amount fall between ¼ and ½ mil of the parameter making it a “**Concern**” violation. Anything else is deemed “**Critical**”.

The screenshot shows the 'Violation Checklist Report' window with the 'Adjust Violation Range' dialog box open. A red arrow points to the 'Adjust Violation Range' button in the report window. A dashed red line connects this button to the dialog box. The dialog box shows a table for adjusting violation ranges for various types like Padstack, Circuit Violation, etc., with columns for Concern and Tolerance values.

Violation Type	Concern	Tolerance
Padstack	0.0005	0.00025
Circuit Violation	0.0005	0.00025
Board Edge Violation	0.0005	0.00025
Soldermask Violation	0.0005	0.00025
Silkscreen Violation	0.0005	0.00025
Test Assembly Violation	0.0005	0.00025
Design Integrity Violation	0.0005	0.00025
Component Violation	0.0005	0.00025

Violations can be **sorted** by selecting the column button above each data column. First selection sorts high to low, second sorts low to high, third sorts high to low again...

Check all boxes on for a violation type to **Delete** or **Save** from list

The screenshot shows the 'Violation Checklist Report' window. At the top, there is an 'Adjust Violation Range' button and a 'Violation File:' field containing './my_violation_file.vio'. Below these are 'Save Violation File', 'Read Violation File', and 'Browse' buttons. A section titled 'Choose Violations to View...' contains radio buttons for 'Critical', 'Concern', and 'Tol', with 'Tol' selected. A table with columns: Param, Layer, Seq, Violation Type, and Comment is displayed. The table contains several rows of violation data. A red circle highlights the first three columns of the table, and a red arrow points to the 'Save Violation File' button. At the bottom, there are buttons for 'Delete Selected Violations', 'Clear Accepted Violation File', 'Close Violation Checklist', and 'Save Violation Summary Report'. A red arrow points to the 'Save Violation Summary Report' button.

Param	Layer	Seq	Violation Type	Comment
12	0	0	Thermal Leg Connection - Min Qty	
12	0	0	Thermal Leg Connection - Min Qty	
7	0	0	Annular Ring - Via Hole	
7	0	0	Annular Ring - Via Hole	
7	0	0	Annular Ring - Via Hole	
7	0	0	Annular Ring - Via Hole	
7	0	0	Thermal Leg Connection - Min Qty	
4	0	0	Annular Ring - Via Hole	
2	0	0	Annular Ring - Other	
4	0	0	Annular Ring - Other	

Creates a text summary report of all DRC violations. These violations are itemized by violation amounts and sorted by type. Creation of the file can be either in ASCII ".txt" file format or in a comma-delimited spreadsheet-ready format.

Empties all data contained in the "approved.vio" file. All **Accepted** violations are returned to the **Violation Checklist** for review or deletion.

This column shows the checking sequence which is the order the checks were performed

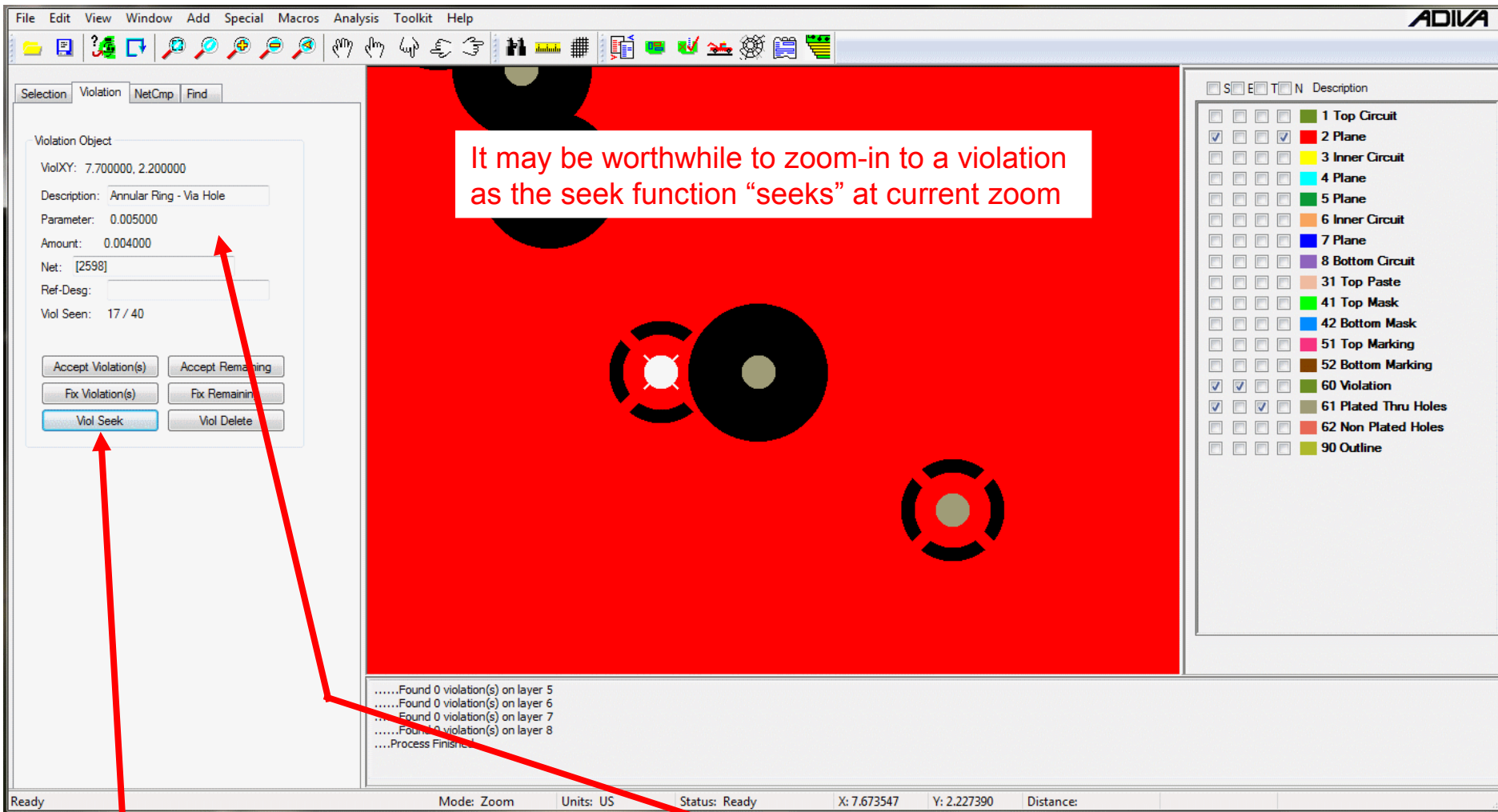
Adjust Violation Range

Violation File:

Choose Violations to View...

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Accepted	Param	Layer	Seq	Violation Type	Comment
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	0	10	Annular Ring - Via Hole	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	4.00000	2	33	Thermal Leg Connection - Min Qty	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	4.00000	4	34	Thermal Leg Connection - Min Qty	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	0	4.00000	7	36	Thermal Leg Connection - Min Qty	Need to Review Again
<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	4.00000	5	35	Thermal Leg Connection - Min Qty	Rvwd - 1 accepted
<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	2	17	Annular Ring - Via Hole	Rvwd - 1 accepted
<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	4	18	Annular Ring - Via Hole	Rvwd - 1 accepted
<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	7	20	Annular Ring - Via Hole	Rvwd - 1 accepted
<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	5	19	Annular Ring - Via Hole	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0	0.00500	2	21	Annular Ring - Other	

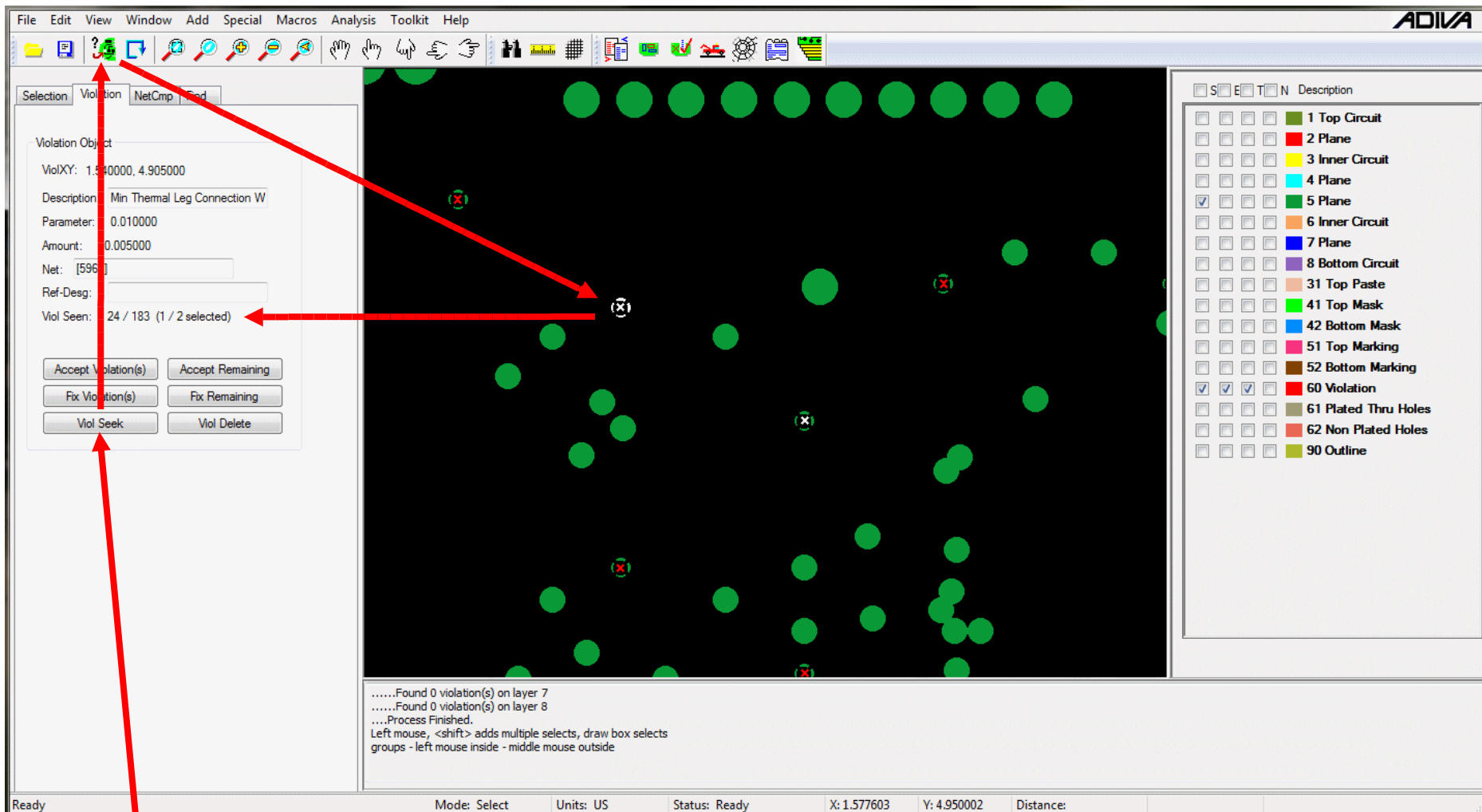
Comments can be added to the checklist and saved to a Violation file. Enter any text and save the violation file – when the violation file is reloaded, these comments will display as they were entered



Violation details are shown here

Once a Violation Type is chosen for review, select **Viol Seek** to review graphically the violations selected **<shift>Viol Seek** progresses backward

NOTE: Worst violations are always shown first



Individual or groups of violations can also be reviewed. **ViolSeek** to the first violation type selected in the **Violation Checklist**, choose the **Select** button then click on an individual violation or window-select a group of violations to review. Notice the **ViolSeen** list shows the qty selected

Read information on the one violation selected – or - **ViolSeek** again to review the group items selected. Choose **Select** again to un-select violations.

A violation (or group of violations) can be **Accepted** which removes the violation(s) from the “violation seek” list.

The violation(s) is(are) not removed – just marked so that the violation(s) is(are) not seen. Notice the violation count shown in the Violation Checklist adjusts to a lower number while the count for the **Accepted** violation(s) increases.

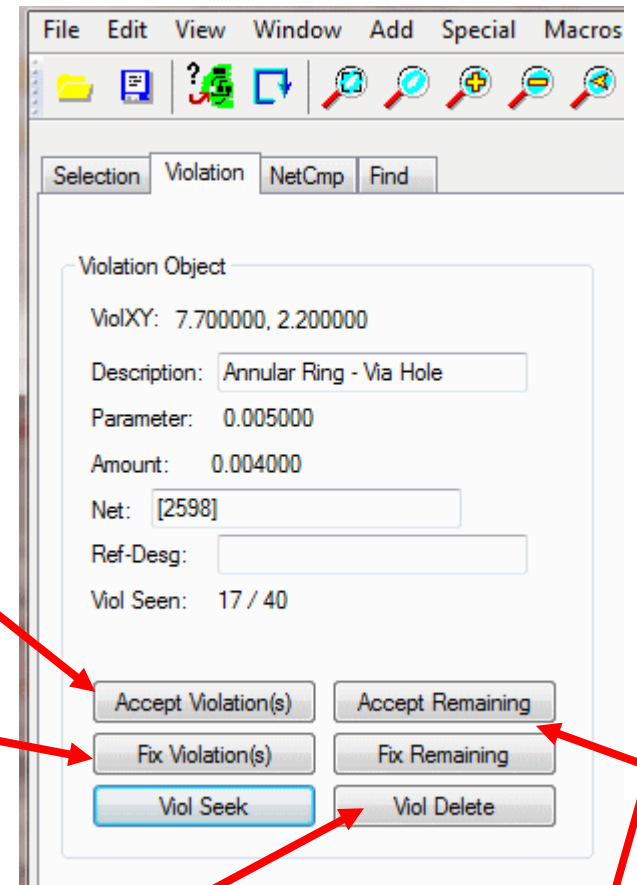
An “approved.vio” file is created in the DRC project directory containing accepted violations. This file can be used in future DRC analysis to filter already approved violations from a new design.

A violation (or group of violations) can be **Fixed** which creates a file in the DRC project directory called “fix.vio”.

This file is typically a collection of violations that a reviewer is interested in having someone else review or fix the violation in a CAD system.

The “fix.vio” file can be read into specific CAD systems or read back into Adiva’s **Violation Checklist** to review only the violations to be “fixed”.

A violation (or group of violations) can be **Deleted** removing it from the Violation Checklist results list.



Fixing or Accepting the Remaining violations adds the currently viewed violation and all those left to be seen into their appropriate .vio files

Violations can also be saved in a format suitable for web-browser display

Select the **DRC Archive** Icon for web image creation



A **DRC Archive** dialog will appear...

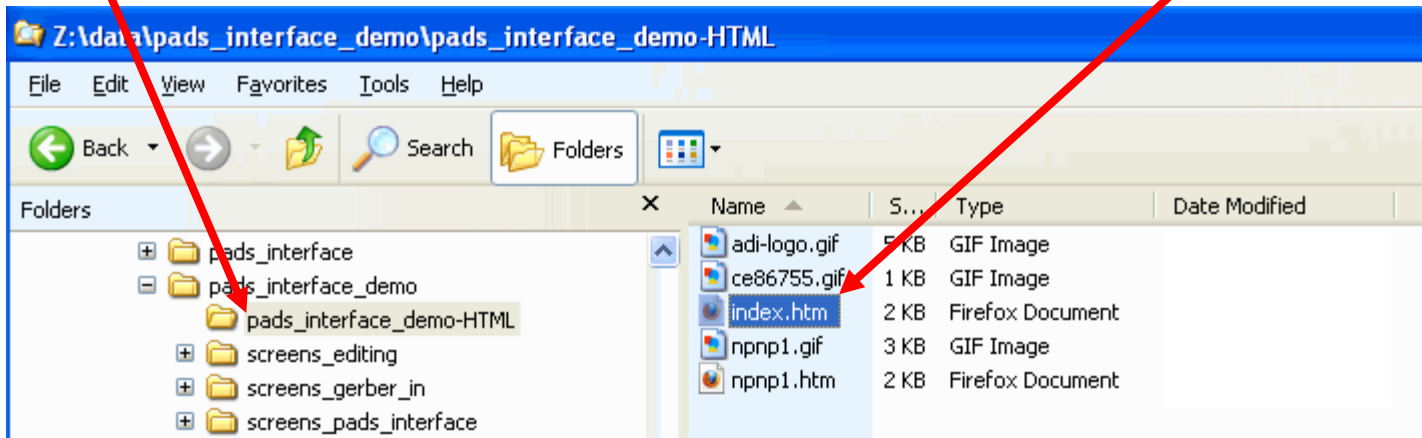
Fill in items such as part number, revision, designer's and checker's name if desired then...

Add any custom notes to help communicate the issue...

Select **Create** to finish the **DRC Archive**

Leave this dialog open and select **Create** for other violations to be archived

To view violations that have been archived to HTML, navigate through **Windows Explorer** finding the Adiva HTML directory (should be under the main job directory) and double-click on “**index.htm**”....



A web browser should open displaying a matrix of violations that have been archived.

Violations should be clearly described – click on one to see a graphic of the violation

Design Analysis Archive

	Adiva Corporation		Part No. 123_23ASB		Rev. AA		Last Update:		
	Designer: Designer		Checked: Checker		Orig Date:				
Padstack	Circuit	Board Edge	Silk & Mask	Test & Assembly	Design Integrity	Signal Integrity	Component	Reference	Net Compare
Min Non-Plated Hole to Non-Plated Hole1									

Web browser should now show a graphic of the selected violation including specific details about the violation...

Violation Description,
Check parameter,
Violation amount,
XY location,
Layer involved

Custom note
added from main dialog

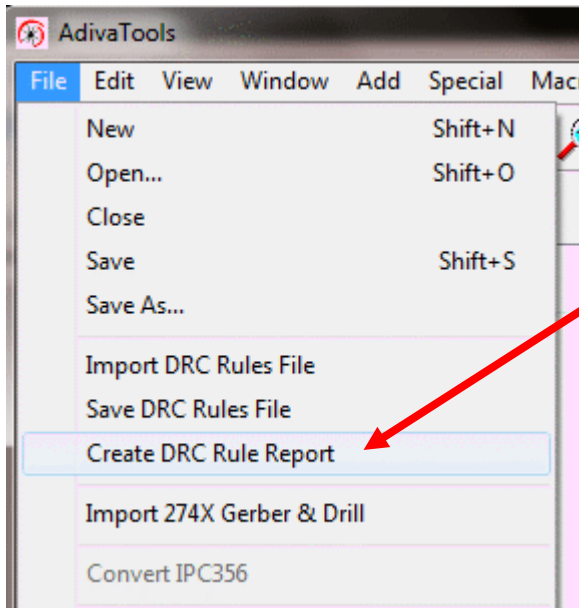
Same graphic displayed
in AdivaTools DRC Violation
review

The screenshot shows a Mozilla Firefox browser window titled "DRC Design Analysis Report". The page content includes a header "Design Analysis Archive" and a link "Return to Index Page". Below this is a table with the following data:

	Adiva Corporation	Part No. 123_23ASB	Rev. AA	Orig Date:
Violation Type	Amount - Inches	Parameter - Inches	X - Y Location	Layer
Min Non-Plated Hole to Non-Plated Hole-1	0.01850	0.05000	X:0.50100 Y:2.49340	252 (Non Plated Holes),

Below the table is a custom note: "These Non-Plated Holes are too close...". At the bottom of the report is a graphic showing a grid of holes on a PCB. The holes are represented by red circles and red 'X' marks. Two white circles are also present, indicating the specific location of the violation.

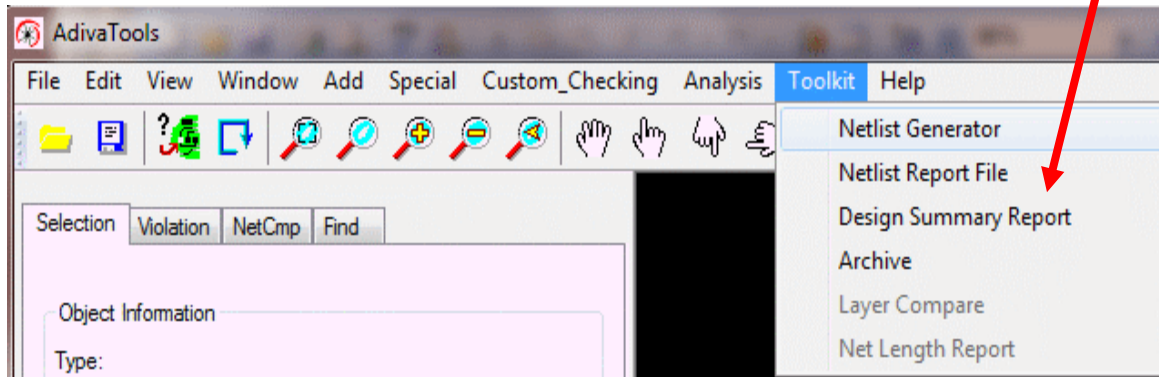
Extra DRC Outputs



Select **File > Create DRC Rule Report** to create an ASCII text file documenting all of the DRC Check dialogs. In this document will be a listing of all DRC Check settings, their values and whether they are on/off.

This is useful in documenting the settings of all DRC checks for later reference.

Select **Toolkit > Design Summary Report** to receive an ASCII text file in comma-delimited (spreadsheet ready) format summarizing details about the design.



Included in this report is enough information suitable for characterizing the design including items such as board dimensions, hole counts, min spacing values, etc...

END
PADS to ADIVA
Interface
(Quick-Start User Guide)