ADIVA Gerber / Drill Input (Quick-Start User Guide)

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Notice

Representations in this User Guide are meant as an overview and quick reference. Full details can be found in the On-Line manuals located at the *ADIVA Corporation* website - www.adiva.com

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Step 1 Generic Gerber and Drill Input

- Translator will accept 274X Gerber along with Drill files in Excellon format
- Drill files in Cadence Allegro, Mentor Boardstation, Mentor Expedition, Altium, Mentor Pads, Zuken are also accepted.
- Place all files into a single directory.
- Start AdivaTools simply by double-clicking the AdivaTools icon on the Windows Desktop

Start by double-clicking the **AdivaTools** desktop icon to start the application and provide access to the menus shown below...



A new dialog will open listing all of the files selected from the previous dialog.

This is a good time to review the list and make sure all of the files intended to be converted are on the list – if not, **Cancel** and start over.



Assign layer numbers to each file on the list.

Number assignment should follow some reasonable order for clarity.

For example, The design's Top Circuit should be layer # 1 and so on...

Choose a layer type for each file.

/

This is important for later processing. ADIVA needs to know which is the Top Circuit, Outline, Plated Holes, etc....

iport 274X Gerber (8 Drill					
Units US 💌						
ilename	File Format	Offs	et X Offset Y	Layer	# LayerType Data Format	
b_outline.pho	274×	• 0.0	000 0.0000	90	Outline 🗸	
l1_gerber.pho	274×	• 0.0	000 0.0000	1	Inner Circuit	
l2_gerber.pho	274×	• 0.0	000 0.0000	2	Bottom Circuit	
I3_gerber.pho	274×	• 0.0	000 0.0000	3	Outline Internal Cut Outla	
I4_gerber.pho	274×	• 0.0	000 0.0000	4	Top Mask	
I5_gerber.pho	274×	• 0.0	000 0.0000	5	Top Marking	
l6_gerber.pho	274X		000 0.0000	6	Bottom Marking None	
pmb_gerber.pho	274X	0.0	000 0.0000	32	Top Paste Bottom Paste	
pmt_gerber.pho	274X	0.0	000 0.0000	31	Top Comp Outline Bottom Comp Outline	
smb_gerber.pho	274×	0.0	000 0.0000	34	Top Place Boundary Bottom Place Boundary	
smt_gerber.pho	274×		000 0.0000	33	Top KeepOut	
ssb gerber.pho	274×			136	Fab. Drawing	
					Assy. Drawing	

Convert

Cancel

Some files may need to be offset for alignment purposes. If this offset value is known, it can be entered in the spaces provided. Values are in inches or mm and a negative offset is defined with the minus (-) sign.

				\bigwedge		Note: if ar later edite	n offset value is not known, the data car ed to bring everything into alignment.
port 274X Gerber & D	rill						
Units US 💌	File Format	ſ)ffset X	Offset Y	Layer	# LayerType	Data Format
b_outline.pho	274×	*	-1.000	-1.000	90	Outline	
l1_gerber.pho	274×	~	0.0000	0.0000	1	Top Circuit 🛛 🗸	
l2_gerber.pho	274×	*	0.0000	0.0000	2	Inner Circuit 🔽	
l3_gerber.pho	274×	*	0.0000	0.0000	3	Inner Circuit 🔽	
l4_gerber.pho	274×	~	0.0000	0.0000	4	Inner Circuit 🔽	
l5_gerber.pho	274×	~	0.0000	0.0000	5	Inner Circuit 🔽	
l6_gerber.pho	274×	~	0.0000	0.0000	6	Bottom Circuit 🛛 🗸	
pmb_gerber.pho	274×	~	0.0000	0.0000	32	Bottom Paste 🔽	
pmt_gerber.pho	274×	~	0.0000	0.0000	31	Top Paste 🔽	
smb_gerber.pho	274×	~	0.0000	0.0000	34	Bottom Mask 🛛 🗸	
smt_gerber.pho	274×	~	0.0000	0.0000	33	Top Mask 🔽	
lash gathar pha	274X	~	0.0000	0.0000	36	Bottom Marking 🛛 🗸	
ssb_gerber.prio							

Convert

Cancel

Top half of a completed file import list. Note the Layer number and layer type assignments									
Units US 💌									
Filename	File Format	C)ffset X	Offset	Layer	# LayerType		Da	
b_outline.pho	274×	*	0.0000	0.0000	90	Outline	~		
l1_gerber.pho	274×	*	0.0000	0.0000	1	Top Circuit	~		
I2_gerber.pho	274×	*	0.0000	0.0000	2	Inner Circuit	~		
I3_gerber.pho	274×	*	0.0000	0.0000	3	Inner Circuit	~		
I4_gerber.pho	274×	~	0.0000	0.0000	4	Inner Circuit	~		
l5_gerber.pho	274×	~	0.0000	0.0000	5	Inner Circuit	~		
l6_gerber.pho	274×	~	0.0000	0.0000	6	Bottom Circuit	*		
pmb_gerber.pho	274×	~	0.0000	0.0000	32	Bottom Paste	*		
pmt_gerber.pho	274×	~	0.0000	0.0000	31	Top Paste	~		
smb_gerber.pho	274×	~	0.0000	0.0000	34	Bottom Mask	*		
smt_gerber.pho	274×	*	0.0000	0.0000	33	Top Mask	~		
ssb_gerber.pho	274×	*	0.0000	0.0000	36	Bottom Marking	*		
sst gerber.pho	274X	¥	0.0000	0.0000	35	Ton Marking	¥		
Convert Cancel]								

Bottom half of a completed file import list. Note the Drill file format choices, layer type, data format and drill tool assignment files

		/			
🔲 Import 274X Gerber & Drill					
Units US 💌 Filename F	File Format Offet X	Offset Y Layer	# LayerТуре	Data Format	
[4_gerber.pho	274× 🗸 0.0000	0.0000 4	Inner Circuit 🛛 💌		<u>^</u>
l5_gerber.pho	274× 🗸 0.0000	0.0000 5	Inner Circuit 🔽		
l6_gerber.pho	274X 0.0000	0.0000 6	Bottom Circuit 🛛 🗸		
pmb_gerber.pho	274X 🖌 0.0000	0.0000 32	Bottom Paste 🔽 🗸		
pmt_gerber.pho	274X 🗸 0.0000	0.0000 31	Top Paste 🔽		
smb_gerber.pho	274X 🔽 0.0000	0.0000 34	Bottom Mask 🛛 👻		
smt_gerber.pho	274X 🔽 0.0000	0.0000 33	Top Mask 🛛 👻		
ssb_gerber.pho	274X 🔽 0.0000	0.0000 36	Bottom Marking 🛛 👻		
sst_gerber.pho	274X 🔽 🔽 0.0000	0.0000 35	Top Marking 🛛 🖌	↓ ↓	
drl. drl	Mentor Pads 🛛 🗸 0.0000	0.0000 50	Plated Thru Holes 🛛 🖌 2	🗸 4 🔽 T 🔽 A 🔽 Create 🛛 Browse drl.rep	
drl_npt.drl	Mentor Pads 🛛 🖌 0.0000	0.0000 51	Non Plated Holes 🛛 🖌 2	🖌 4 🔽 T 🔽 A 🔽 Create 🛛 Browse drl_npt.rep	p la
Convert Cancel					
When everything is a	Data for 2=leadir defined.	mat fields ng digits 4	s (in this case 2 4 =trailing digits T L	T A) mean =trailing suppression A=abso _=leading suppression I=incre	olute reference emental reference

select Convert to build the ADIVA database



Step 2

Layer Description

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Next, if the **Layer Description** dialog is not already open then under the **Special** menu choose **Layer Description**.

Even though layers were defined earlier, there is more detail required to fulfill needs associated with DRC checks, Netlist Compare, etc...

Initial opening of the Layer Description dialog will look like the below image....

Adjustments may need to be made to further define layers

Note that the below image shows Z-Position values all set to zero. In certain cases, these values will be automatically defined such that each layer is 10 mils apart. This is a standard default value and should only need to be modified if the user has exact values to enter. More details regarding Z position are on the next page...

🔲 Layer De	escription						
Layer	Layer Type		Polarity		Z-Position	Copper Thickness	
1	Top Circuit	~	Positive	*	0.000000	0.000000	^
2	Inner Circuit	~	Positive	~	0.000000	0.000000	
3	Inner Circuit	~	Positive	~	0.000000	0.000000	
4	Inner Circuit	~	Positive	~	0.000000	0.000000	
5	Inner Circuit	*	Positive	~	0.000000	0.000000	
6	Bottom Circuit	~	Positive	~	0.000000	0.000000	
31	Top Paste	~					
32	Bottom Paste	~					
33	Top Mask	~					
34	Bottom Mask	~					
35	Ton Marking	v					~
Update	Cancel						

Z-Position defines the stackup – layer to layer dimension referenced from the top layer which should always be "0".



If Buried / Blind Vias or Back Drills are used in a design, then it is the **Layer Description** dialog that defines the start and end drill mapping for the drills.

The value entered is the Z-Position value assigned to the layers involved - it is **<u>NOT</u>** the layer number.

Layer Des	cription				
Layer	Layer Туре	Polarity	Z-Position	Copper Thickness	
6	Bottom Circuit 🛛 👻	Positive 💌	60	0.000000	^
31	Top Paste 💌				
32	Bottom Paste 💌				
33	Top Mask 💌				
34	Bottom Mask 😽 👻				
35	Top Marking 😽 😽				
36	Bottom Marking 🛛 👻				
50	Plated Thru Holes 🛛 👻				
51	Buried Vias 💌		0.000000	30.00000	
90	Outline 🗸		7	1	
		/			~
Update	Cancel				

This is the Z-Position of the start layer This is the Z-Position of the end layer

Step 3 Database Preparation - Editing

With a built database, there may be several other functions that need to be completed to prepare a design for DRC analysis. These functions may require some light editing of the data. They include....

Layer Alignment Board Outline creation Splitting Non-Plated Holes away from Plated Holes onto their own layer Removing Title Blocks, Coupons, etc

If this is the case, reference the **ADIVA Data Editing Guide** for details on how to edit for these requirements.

Then continue the process of prepping data for analysis....

Step 4

Gerber Netlist Extraction



Select Netlist Generator from Toolkit Menu

When netting of Gerber is complete, "Process Finished" will be displayed in message box

Filter ✓ Pads All ✓ Lines ✓ Arcs ✓ Polygons ✓ Apertures ✓ Classes	の高速		
1 c10.000000 2 c5.000000 3 c15.000000 4 c25.000000 5 c8.000000 6 r13.000000x13.000000 7 r50.000000x50.000000 8 r16.000000x16.000000 9 r24.000000x24.000000			
10 r30.00000x30.00000	Adding positive object: Writing Nets (0 Power/Ground Net	s s - 788 Signal (Nets.)	- Finishad
Snap: Off 🛛 🗸 Separation: Edge 🗸	Netting: ** Normai Ter	mination **Proces	s rinisnea.
Ready	Mode: Select	Units: US	Status: Ready

Step 5

Netlist Compare (See the ADIVA CAD Netlist Comparison Guide for further details of this process)

🛞 AdivaTools	ect the NetCmp tab
Eile Edit View Window Add Special Macros Analysis Toolkit Sig	
Selection Violation NetCmp Find	Browse and select the "net.crf" file for this job
Net Compare Cad Netlist File: a\pads_interface_demo\net.crf Execute	 Execute the Net Compare Routine
Net Compare Summary Unmatched CAD Points: Duplicate CAD Points: Broken Nets: Shorted Nets: Report File: Save	AdivaTools Ele Edit View Window Add Special Macros Analysis Toolkit Sig Ele Edit View Window Add Special Macros Analysis Toolkit Sig Selection Violation NetCmp Find Net Compare Cad Netlist File: a\pads_interface_demo\net.crf Browse Execute Net Compare Summary Unmatched ADIVA Points: 0 Duplicals CAD Points: 0 Duplicals CAD Points: 0 Broken Nets: 6 Beoott File:

Step 1: Choose the Summary Item to Review

Step 2: Scroll to Review Problems and select one to see





Uncheck All Summary Items to "exit" Net Compare

Step 6

Pad / Hole Definition

Adds Pad "FUNCTION" Intelligence to Database

Pad / Hole Definition needed to identify Pad and Hole types so that various checks can be run accurately

ile Edit View Window Add Special Custom	Checking Analysis Toolkit Help	
😑 🖪 🍕 🔽 🖓 🖓 🔁 🦉	දුණා දුණා Pad-Hole-Definition	
	DRC - Pad Stack	
Selection Violation NetCmp Find	DRC - Circuit	
	DRC - Board Edge	
Object Information	DRC - Solder mask	
Туре:	DRC - Silkscreen	
Count:	DRC - Test Assembly	
Net:	DRC - Design Integrity	
Ref-Desg.	DRC - Group Execute	
Aperture:		~
	Violation Checklist	Ctrl+X
Layer.	DRC Include/Exclude Area	Ctrl+W

Select Analysis > Pad-Hole Definition to start the function...

Review the "stackups" that are created by zooming in on Layer 1 And selecting the "Seek" button for each Padstack Type. Watch the screen jump to the next "seek"

NOTE: Only 1 or 2 "seeks" per padstack type is needed to determine if the Default choice is correct.

Do a quick glance at each one, adjust if needed (usually not needed) then move on to the next one – don't let this process take more than a few minutes!

Pad Hole D	efinition						×	
Hole Size	Plating	TopPad Size	BotPad Size	QTY	Class			If default choice requires
c10.00	P	c20.000000	c20.000000	351	V 🗸	Seek 🌅		adjustment, adjust as needed
c10.00	P	c23.000000	c23.000000	480	V 🗸	Seek		to one of the following options
c12.00	P	c30.000000	c30.000000	777	V 🗸	Seek		V = Via
c12.00	P	r122.000000x1	c30.000000	1	V 🗸	Seek		S = SMT
c12.00	P	c50.000000	c30.000000	1	V 🗸 🗸	Seek		P = Pin - Thru hole
c138.00	P	c315.000000	c315.000000	1	Р 🗸	Seek		C = Cosmetic (no real function)
c15.00	P	c35.000000	c35.000000	13	V 🗸	Seek		t = test point
c213.00	P	c330.000000	c330.000000	4	Р 🗸	Seek		T = Non-Plated Hole
c31.50	N	c3.940000	c3.940000	40	T 🗸	Seek		F = fiducial
c37.40	N	c3.940000	c3.940000	4	Т 🗸	Seek		
c39.37	N	c20.000000	c20.000000	1	Т 🗸	Seek		Select Annly to finish routine
c39.37	Р	c70.870000	c70.870000	10	p v	Seek 🗸 🗸		
Apply	Cancel							

Step 7

Load DRC Check Rules (See ADIVA Running DRC Checks Guide for more details)

66 A	diva	Tools							
File	<u>E</u> dit	⊻iew	<u>W</u> indow	Add	Special				
N	<u>N</u> ew Shift+N								
Open Shift+O									
⊆lose									
Save Shift+S									
Sa	ave <u>A</u> s								
Import DRC Rules File									
Save DRC Rules File									
Create DRC Rule Report									
In	nport 2	274X Ge	erber & Dri	I					
0	onvert	IPC35	6						
Ð	rint			Shift	t+P				
Pr	rint Pre	e <u>v</u> iew							
Pį	rint Sel	tup							
R	ecent I	File							
E	<u>×</u> it								

Select File > Import DRC Rules to bring in a master set of rules that you may have created.

Typically these are stored in the c:\adiva\data directory

In this case, load a file called "**95_example.rul**" which is a basic set of IPC rules and industry standards that ADIVA supplies with all installations.

You can skip this function if all you need to do is set a few rules in a menu and run checks.... The DRC check menus will appear blank ready for value entries.

Step 8

DRC Checks (See ADIVA Running DRC Checks Guide for more details)

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	PadStack Checklist	
Check ON layers to review	Areas Whole Layer Resolution 1/4 Mil	
Check ON checks to run	Check By Layer Outer Positive Layers Layers Top Circuit 1 All On/Off Annular Ring - Pin-Thru Hole 0.005 Annular Ring - Other 0.005	Inter Positive Layers All On/Off No Copper Required ✓ Annular Ring - Pin-Thru Hole 0.005 ✓ Annular Ring - Via Hole 0.005 ✓ Annular Ring - Other 0.005
Values are in inches or mm 5-mil space = 0.005 value	Negative Law Mail On/Off Annular Ring - Pin-Thru Hole Annular Ring - Via Hole Annular Ring - Other Annular Ring - Other Copper and Anti-Pad Clearance to Plated Hole Thermal Leg Connection - Min Qty Min Thermal Leg Connection Width Min Thermal Leg Length	Layers
Execute to start checks	Execute Update Cancel	

s Whole Layer Resolution 1/4 Resolution 1/4	Mil 👻			
Inner NegPlane				
Outer Positive Layers				
Layers				
V Top Circuit 1 V Bottom Cir	rcuit 8			
All On /Off				
	0.004	Min SMT to SMT	0.004	
Min Trace to Pad	0.004	Min SMT to SMT (Same Net)	0.004	
Min Trace to ViaPad	0.004	Min ViaPad to ViaPad	0.004	
Min Trace to SMT	0.004	Min ViaPad to SMT	0.004	
Min Trace to TestPad	0.004	── ✓ Min ViaPad to SMT (Same Net)	0.004	
📝 Min Pad to Pad	0.004	Min ViaPad to TestPad	0.004	Some checks do
Min Pad to Pad (Same Net)	0.004	📝 Min TestPad to TestPad	0.004	use mils for a val
📝 Min Pad to ViaPad	0.004	🕼 Min TestPad to SMT	0.004	
Min Pad to TestPad	0.004	☑ Min TestPad to SMT (Same Net)	0.004	This is pixels
Min Pad to SMT	0.004	Min Back-Drill to Trace	0.012	
Min Pad to SMT (Same Net)	0.004	Min Back-Drill to Pad (any type)	0.012	This is degrees
Min Copperto Fiducial	0.02	📝 Min Trace Width	0.004	This is degrees
Min Fiducial Barrel	0.02	Min Trace Connection Width		
Min Copper to Board Edge	0.02	Min Resist Sliver	0	
Min Trace to Non-Plated-Hole	0.02	Min Acid Trap 📝 Traces Only	3	
Min Pad (any type) to Non-Plated-Hole	0.02	Min Trace Angle	135	

Step 9

Violation Review (See ADIVA Running DRC Checks Guide for more details)

The Violation Checklist appears when checks are completed

The Checklist can also be opened while checks are running by selecting its Toolbar Icon

	👝 🗉 🌿 🗗 🔎 🔎 🔎 🖉 🖑 🖑 🎣 🤤 🐨 🚻 🚥 🗰 🎽 🖬 🛥 🥙 🗮 🧮 🗒														
	Violations are displayed by concern level														
	as defined by the range setting														
P	Viola	ation Che	cklist Report												
	Τ														
		Adjust V	iolation Range		Violation File	olation File: ./my_violation_file.vio									
				_		Save V	iolation File		lead Violation File Browse						
	Choose Violations to View														
		Critical	Concem	🗖 Tol	Accepted	Param	Layer	Seq	Violation Type	Comment					
Γ		12				4 00000									
		12		0	0	4.00000	4	34 36	Thermal Leg Connection - Min Qty						
		7			0	0.00500	2	17	Annular Ring - Via Hole						
		7		0	0	0.00500	4	18	Annular Ring - Via Hole						
		7		0	0	0.00500	7	20	Annular Ring - Via Hole						
	1	7	0	0	0	4.00000	5	35	Thermal Leg Connection - Min Qty						
	~	4	0	0	0	0.00500	5	19	Annular Ring - Via Hole						
1		2	0	0	0	0.00500	2	21	Annular Ring - Other						
L		2	0	0	0	0.00500	4	22	Annular Ring - Other	•					
ſ	Del	ete Selecte	d Violations	Clear Accen	ted Violation F	ile									
ſ	_														
	Clo	ose Violatio	n Checklist	Sure Vielatio	o Summary Re	port									
	S 01152														

Choose a **Violation Type** and amount to review by using **ViolSeek** on the main user interface Select Close Violation Checklist to close the dialog (violations are not lost) Copyright © 2021 – Adiva Corporation Adjusting the **Violation Range** effects violation count distribution in the **Violation Checklist**. The values listed for each range analyze how close a violation comes to the parameter to determine the category a particular violation will be placed. Changes take effect on **Update**.

For example.... given the range values shown, if a check parameter is 0.005 and the violation amount is 0.00480 - this violation amount falls within $\frac{1}{4}$ Mil of the parameter categorizing the violation as "**Tolerance**". If the violation amount is 0.0046 - this makes the violation amount fall between $\frac{1}{4}$ and $\frac{1}{2}$ mil of the parameter making it a "**Concern**" violation. Anything else is deemed "**Critical**".

					Adjust Violation Rang	ye .	
Violation Checkli Report		-			Value Within Parameter		
Adjust Violation Range Violation F	ile: /mv_viola	tion file vi	0	_	Violation Type	Concern	Tolerance
					Padstack	0.0005	0.00025
Channe Mederland to Menu	Save Vic	plation File	Read Violation File	Bro	Circuit Violation	0.0005	0.00025
	d Prom		Sag	Vie	Board Edge Violation	0.0005	0.00025
				VI0	Soldermask Violation	0.0005	0.00025
	4.00000	4	34 Thermal Leg Conn	nectio	Silkscreen Violation	0.0005	0.00025
	4.00000	7	36 Thermal Leg Conne 17 Annual Bing Man	nection	Test Assembly Violation	0.0005	0.00025
	0.00500	4	17 Annular Ring - Via 18 Annular Ring - Via	Hole	Design Integrity Violation	0.0005	0.00025
	0.00500	7	20 Annular Ring - Via	Hole	Component Violation	0.0005	0.00025
7 0 0 0	4.00000	5	35 Thermal Leg Conn	nectio		0.0000	0.00020
	0.00500	5	19 Annular Ring - Via 21 Annular Ring - Oth	Hole			
	0.00500	4	22 Annular Ring - Oth	her	Update Cancel		
Delete Selected Violations	o File			٦.		_	
Close Violation Checklist Save Violation Summary I	Report						

Violations can be **sorted** by selecting the column button above each data column. First selection sorts high to low, second sorts low to high, third sorts high to low again...

Check all boxes on for a violation type to Delete or Save from list												
Violation Ch	ecklist Report	1										
Adjust	Nolation Range ose Violations to	e View	Violation File	: _/my_viol Save Vi	ation_file.v	/io	ead Violation File Browse					
Critical	Concer	m 🗖 Tol	Accepted	Param	Layer	Seq	Violation Type	Comment				
12			0	4.00000	4	34	Themal Leg Connection - Min Qtv					
12			0	4.00000	7	36	Thermal Leg Connection - Min Qty					
177			0	0.00500	2	17	Annular Ring - Via Hole					
1.177-		0	0	0.00500	4	18	Annular Ring - Via Hole					
7	0	0	0	0.00500	7	20	Annular Ring - Via Hole					
7	0	0	0	4.00000	5	35	Thermal Leg Connection - Min Qty					
4	0	0	0	0.00500	5	19	Annular Ring - Via Hole					
.2	0	0	0	0.00500	2	21	Annular Ring - Other					
	0	0	0	0.00500	4	22	Annular Ring - Other					
Delete Selected Violations Clear Accepted Violation File Close Violation Checklist Save Violation Summary Report												
							Emotios all data contain	ad in the				

Creates a text summary report of all DRC violations. These violations are itemized by violation amounts and sorted by type. Creation of the file can be either in ASCII ".txt" file format or in a comma-delimited spreadsheet-ready format. Empties all data contained in the "approved.vio" file. All **Accepted** violations are returned to the **Violation Checklist** for review or deletion.

This column shows the checking sequence which is the order the checks were performed

💽 Viola	tion Chec	klist Report							
6	Adjust Vi	olation Range		Violation File	./my_viol	ation_file.v	np P	ead Violation File Browse	
	Choose	Violations to Vi	ew				ł		
	Critical	Concern		Accepted	Param	Layer	Seq	Violation Type	Comment
	30	U	U		0.00000	•	10	Annalar rung i ni i nila nolo	
	12	0	0	0	4.00000	2	33	Thermal Leg Connection - Min Qty	
	12	O	0	0	4.00000	4	34	Thermal Leg Connection - Min Qty	
	12	V 0	V 0	0	4.00000	7	36	Thermal Leg Connection - Min Qty	Need to Review Again
	6	0	0	1	4.00000	5	35	Thermal Leg Connection - Min Qty	Rvwd - 1 accepted
	6	0	0	1	0.00500	2	17	Annular Ring - Via Hole	Rvwd - 1 accepted
	6	0	0	1	0.00500	4	18	Annular Ring - Via Hole	Rvwd - 1 accepted
	6	0	0	1	0.00500	7	20	Annular Ring - Via Hole	Rvwd - 1 accepted
V	4	0	0	0	0.00500	5	19	Annular Ring - Via Hole	
	2	0	0	0	0 00500	2	21	Annular Bing - Other	•
Dele	ete Selecter se Violatior	d Violations	Clear Accep Save Violation	ted Violation F n Summary Re	ile port				

Comments can be added to the checklist and saved to a Violation file. Enter any text and save the violation file – when the violation file is reloaded, these comments will display as they were entered



Once a Violation Type is chosen for review,

select Viol Seek to review graphically the violations selected <shift>Viol Seek progresses backward

NOTE: Worst violations are always shown first



Individual or groups of violations can also be reviewed. **ViolSeek** to the first violation type selected in the **Violation Checklist**, choose the **Select** button then click on an individual violation or window-select a group of violations to review. Notice the **ViolSeen** list shows the qty selected

Read information on the one violation selected – or - **ViolSeek** again to review the group items selected. Choose **Select** again to un-select violations.

A violation (or group of violations) can be **Accepted** which removes the violation(s) from the "violation seek" list.

The violation(s) is(are) not removed – just marked so that the violation(s) is(are) not seen. Notice the violation count shown in the Violation Checklist adjusts to a lower number while the count for the **Accepted** violation(s) increases.

An "approved.vio" file is created in the DRC project directory containing accepted violations. This file can be used in future DRC analysis to filter already approved violations from a new design.

A violation (or group of violations) can be **Fixed** which creates a file in the DRC project directory called "fix.vio".

This file is typically a collection of violations that a reviewer is interested in having someone else review or fix the violation in a CAD system.

The "fix.vio" file can be read into specific CAD systems or read back into Adiva's **Violation Checklist** to review only the violations to be "fixed".

A violation (or group of violations) can be **Deleted** removing it from the Violation Checklist results list.



Violations can also be saved in a format suitable for web-browser display

Select the DRC Archive Icon for Web Creation

A DRC Archive dialog will appear...



To view violations that have been archived to HTML, navigate through Windows Explorer finding the Adiva HTML directory (should be under the main job directory) and double-click on "index.htm"....

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A web browser should open displaying a matrix of violations that have been archived.

Violations should be clearly described – click on one to see a graphic of the violation

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Web browser should now show a graphic of the selected violation including specific details about the violation...



END ADIVA Gerber / Drill Input (Quick-Start User Guide)

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